REMARKS

I. Introduction

Applicants have carefully reviewed the application in light of the Office Action mailed January 29, 2004. At the time of the Office Action, claims 1-5, 7 and 12-20 were canceled and claims 6, 8-11 and 21-24 were pending in the Application. In response to the Office Action, Applicants have amended claims 6, 21 and 22 so as to further clarify the subject matter of the present invention. Support for the above amendments can be found, for example, on page 16, lines 7-14 and Fig. 4. Also, in regards to the status of application serial number 09/102,166, the application has been abandoned. Applicants respectfully request reconsideration of the pending claims and favorable action in this case.

II. Claim Objections

The Examiner objects to claims 21 and 22 as depending on claim 13, which was previously canceled. Applicants respectfully submit that the foregoing amendments to these claims address and resolve this objection.

III. The Rejection Of The Claims Under 35 U.S.C. § 112

The Examiner rejects claim 8 under 35 U.S.C. §112, 2nd paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention because it recites "the same area." Applicants traverse this rejection on

the grounds that if the scope of a claim would be reasonably ascertainable by those skilled in the art, then the claim is not indefinite, and the failure to provide explicit antecedent basis for terms does not always render a claim indefinite (M.P.E.P. §2173.05(e) and *Ex parte Porter, 25 USPQ2d 1144, 1145(Bd. Pat. App. & Inter. 1992)* and *Bose Corp. v. JBL, Inc., 274 F.3d 1354, 1359, 61 USPQ2d 1216, 1218-19 (Fed. Cir. 2001)*). Here, it is respectfully submitted that those skilled in the art would clearly understand that the phrase "...are the same area" refers to the recited "said second area" and "said third area." The specification also makes this point clear as set forth, for example, on page 4, lines 12-16, page 16, lines 15-27 and Fig. 4. As the claim would be readily understandable by one of skill in the art, it is respectfully submitted that the foregoing claim is in compliance with the requirements of 35 U.S.C. § 112, 2nd paragraph, and overcomes the pending rejection.

IV. The Rejection Of Claims 6 and 24 Under 35 U.S.C. § 102

Claims 6 and 24 were rejected under 35 U.S.C. § 102(e) as being anticipated by USP No. 5,968,160 to Saito. For the reasons set forth below, it is respectfully submitted that the pending claims are not anticipated by Saito.

First, it is noted that anticipation under 35 U.S.C. § 102 requires **each and every** (emphasis added) element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade*

Commission, 808 F.2d 1471 (Fed. Cir. 1986). For the following reasons, it is submitted that Saito does not anticipate claim 6 nor any claim dependent thereon.

Turning to the pending claims, independent claim 6 recites a data processing method comprising the steps of: writing a processing specification information in a **first area** corresponding to a **first word line** within a **semiconductor device** comprising at least one memory array and a data processor coupled to said at least one memory array through at least one internal data bus; writing data to be processed in a **second area** corresponding to a **second word line**, which is different from the first word line, **within said semiconductor device**, transferring said processing specification information through said at least one internal data bus **in a batch** to said data processor; transferring said data through said at least one internal data bus **in a batch** to said data processor; processing said data by said data processor using said processing specification information and **writing resultant** processed data through said at least one internal data bus **in a batch** in a **third area** corresponding to a **third word line** within said semiconductor device; and obtaining said resultant processed data by reading said third area after **writing** said resultant processed data.

In contrast, Saito discloses an instruction cache and a data cache for holding instruction and data separately from each other. The instruction cache B1 and data cache B2 each include a multi-port cache which is assumed to have n address input ports and n input/output ports.

However, **Saito does not provide any information on the word line processing or disclosure of different word lines, nor is there provided a semiconductor device where data written is to be processed**, as currently recited by claim 6 of the present invention. The cited prior art only shows an instruction cache and a data cache being operable to carry out instructions and data in parallel or in synchronism (Col. 11, lines 31-34). The word line processing as claimed is neither disclosed nor suggested by the prior art. Saito merely discloses a data processing system for providing parallel operation and establishing synchronism between or among processor elements. Thus, Saito does not disclose a cache having word line within a semiconductor device. In doing so, Saito fails to disclose a first area corresponding to a first word line for writing a processing specification information, a second area corresponding to a second word line different from the first word line for writing data to be processed, and a third area corresponding to a third word line for reading and processing resultant data.

Furthermore, as recited by amended claim 6, data corresponding to a word line that can be accessed within a memory array is transferred in a batch to a data processor through at least one internal data bus within the memory array. For example, the memory controller 4 of Fig. 1 writes data processing specification information in the memory cells in the first area connected with the word line "c" in the memory array "A," so as to transfer the data processing specification information to the data processor 30 in a batch, thereby allowing a large quantity of data to be exchanged between the memory array and the data processor within a short period of

time, and achieving high speed processing.

In contrast, Saito discloses that only the first instruction can be executed, while execution of the second instruction has to wait for the result of execution of the first instruction.(see e.g., col. 11, lines 1-15 and col. 11, line 56-col. 12, line 4). It is respectfully submitted that Saito cannot process the information in a batch as recited by claim 6.

Furthermore, the processor elements described in Saito as alleged by the Examiner are fundamentally different from the data processor illustrated in the present invention. As shown in Fig. 3A and 3B of Saito, **no writing operation** can take place to the instruction cache from the processor elements (Col. 10, lines 19-21). Instructions held at the processor elements are directed to buffer registers and decoded by the decoders, wherein instructions are then read by the register files inside the decoders, and whereon arithmetic operations designated by operation codes of the instructions are executed in parallel on the data read out from the register files (Col. 11, lines 31-55). Results are stored in the register file via the store bus. In contrast, the data processor of the present invention processes the different data processing specification information stored in the memory cells "A" connected with the word line "d" in a batch, and the intermediate data "B" is transferred to the data processor 30. The data processor 30 then processes the intermediate data "B" in accordance with the different data processing specification information, and stores thus-obtained resultant data "C" in the memory cells "A," where overhead for **rewriting** the processing specification is caused in the data processor (page 18, line 9-11). Therefore, since

Saito fails to disclose "processing said data by said data processor using said processing specification information and **writing** resultant processed data," it is respectfully submitted that the rejection to claim 6 is improper because the alleged data processor cannot perform **writing** processing specification information or data to be processed as claimed by the present invention.

As anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), for the foregoing reasons, it is clear that Saito does not anticipate amended 6.

V. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 6 is patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

It is further noted that claim 24 recites that a register is coupled between the first and

second data processor portions. Referring to Saito as shown in Fig. 3-A and 3-B, it is respectfully submitted that the alleged registers are individually located inside the alleged data processors. For example, it is readily shown that D1 and D2 are placed inside A2, and D3 and D4 are placed inside A3. It is noted that if it is found that the register conflict takes place between the processor elements, instruction executed by one of the processor elements is retarded or delayed in order to clear or solve the register conflict (Col. 8, lines 27-30). In contrast, in accordance with the present invention, hyper-wide-bit registers are aligned at the center, left and right sides thereof. By adopting this configuration, the data transfer between the two memory arrays or buses and the data processing can be simultaneously executed (page 22, lines 4-6). For at least the foregoing reasons, it is respectfully submitted that claim 24 is patentably distinct over the cited prior art.

VI. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action marked "Final," Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. Favorable consideration is respectfully requested.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked

the need for a petition for extension of time. The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 50-0417.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 4/23/04

By: _____

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W. , Suite 1200
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087